NOTICE OF REVISION (NOR)

THIS REVISION DESCRIBED BELOW HAS BEEN AUTHORIZED FOR THE DOCUMENT LISTED.

1. DATE (YYMMDD)	Form Approved OMB No. 0704-0188
92/06/19	

2. PROCURING ACTIVITY NO.	
3. DODAAC	

4. ORIGINATOR	b. ADDRESS (Street, City, State, Zip Code)	5. CAGE CODE	6. NOR NO.
	Defense Electronics Supply Center	67268	5962-R190-92
a. TYPED NAME (First, Middle Initial, Last)	Dayton, Ohio 45444-5270	7. CAGE CODE 67268	8. DOCUMENT NO. 5962-88639

9. TITLE OF DOCUMENT	10. REVISION LETTER		11. ECP NO.
MICROCIRCUIT, DIGITAL, FAST, CMOS, OCTAL TRANSPARENT LATCH WITH THREE-STATE OUTPUTS, TTL COMAPTIBLE, MONOLITHIC SILICON	a. CURRENT A	b. NEW B	NA

12. CONFIGURATION ITEM (OR SYSTEM) TO WHICH ECP APPLIES

13. DESCRIPTION OF REVISION

Sheet 1: Revisions ltr column; add "b".
Revisions description column; add "Changes in accordance with NOR 5962-R190-92".
Revisions date column; add "92/06/19".

Sheet 5: Total power supply current, I_{CC}, change condition eight bit toggling - 50% duty cycle to, one bit toggling - 50% duty cycle.

This page has been electronically altered and does not match the original.

14. THIS SECTION FOR GOVERNMENT USE ONLY

a. (X one)		
	X	(1) Existing document supplemented by the NOR may be used in manufacture.
		(2) Revised document must be received before manufacturer may incorporate this change.
		(3) Custodian of master document shall make above revision and furnish revised document.

b. ACTIVITY AUTHORIZED TO APPROVE CHANGE FOR GOVERNMENT	c. TYPED NAME (First, Middle Initial, Last)
DESC-ECC	Tim H. Noh

d. TITLE	e. SIGNATURE	f. DATE SIGNED
for Chief, Custom Microelectronics	Tim H.Noh	(YYMMDD) 92/06/19

15a. ACTIVITY ACCOMPLISHING REVISION	b. REVISION COMPLETED (Signature)	c. DATE SIGNED
DESC-ECC	Joseph A Kirby	(YYMMDD) 92/06/19

REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add vendor CAGE U4637 and 69210. Add case outlines T and U. Change test limits for line regulation, load regulation, standby current drain, and standby current drain with line tests. Change test conditions for line regulation and output voltage tests. Add temperature characterization for ripple rejection test. Change footnotes 1/, 2/, and 5/ in table I.	89-07-24	M. A. Frye

THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED.

REV																			
SHEET																			
REV																			
SHEET																			

A REV STATUS OF SHEET	REV	A	A	A	A	A	A	A	A	A	A	A	A		
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12		

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
Marcia B Kelleher

CHECKED BY
Monica L. Poelking

APPROVED BY
Michael A Frye

DRAWING APPROVAL DATE
88-09-08

REVISION LEVEL
A

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, DIGITAL, FAST, CMOS, OCTAL TRANSPARENT LATCH WITH THREE-STATE OUTPUTS, TTL COMPATIBLE, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	5962-88639

SHEET 1 OF 12

DESC FORM 193
SEP 87

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:

5962-88639	01	R	X
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54FCT573	Octal transparent latch with three-state outputs, TTL compatible
02	54FCT573A	Octal transparent latch with three-state outputs, TTL compatible

1.2.2 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Case outline
R	D-8 (20-lead, 1.060" x .310" x .200"), dual-in-line package
S	F-9 (20-lead, .540" x .300" x .100") flat package
2	C-2 (20-terminal, .358" x .358" x .100") square chip carrier package

1.3 Absolute maximum ratings. 1/

Supply voltage (V_{CC})	-0.5 V dc to +7.0 V dc
Input voltage range 2/	-0.5 V dc to V_{CC} +0.5 V dc
Output voltage range 2	-0.5 V dc to V_{CC} +0.5 V dc
DC input diode current (I_{IK})	-20 mA
DC output diode current (I_{OK})	-50 mA
DC output current	±100 mA
Power dissipation (P_D) 3/	500 mW
Thermal resistance (O_{JC})	See MIL-M-38510, appendix C
Storage temperature	-65°C to +150°C
Junction temperature (T_J)	+175°C
Lead temperature (soldering, 10 seconds)	+300°C

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	+4.5 V dc to +5.5 V dc
Maximum logic low voltage (V_{IL})	0.8 V dc
Minimum logic high voltage (V_{IH})	2.0 V dc
Case operating temperature (T_C)	-55°C to +125°C
Minimum setup time, high or low (D_n to LE) (t_s)	2.0 ns
Minimum hold time, high or low (D_n to LE) (t_h)	1.5 ns
Minimum LE pulse width, high or low (t_w)	6.0 ns

1/ All voltages referenced to GND.
2/ For V_{CC} > 6.5 V dc, the upper bound is limited to V_{CC}.
3/ Must withstand the added P_D due to short circuit test, e.g., I_{OS}.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standard, and bulletin. Unless otherwise specified, the following specification, standard, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standard, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{CC} = 5.0 V dc ±10% unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
High level output voltage	V_{OH}	V_{CC} = 4.5 V V_{IL} = 0.8 V V_{IH} = 2.0 V	I_{OH} = -300 µA	1, 2, 3	All	4.3		V
			I_{OH} = -12 mA	1, 2, 3	All	2.4		
Low level output voltage	V_{OL}	V_{CC} = 4.5 V V_{IL} = 0.8 V V_{IH} = 2.0 V	I_{OL} = 300 µA	1, 2, 3	All		0.2	V
			I_{OL} = 32 µA	1, 2, 3	All		0.5	
Input clamp voltage	V_{IK}	V_{CC} = 4.5 V, I_N = -18 mA		1, 2, 3	All		-1.2	V
High level input current	I_{IH}	V_{CC} = 5.5 V, V_{IN} = 5.5 V		1, 2, 3	All		5.0	µA
Low level input current	I_{IL}	V_{CC} = 5.5 V, V_{IN} = GND		1, 2, 3	All		-5.0	
Short circuit output current	I_{OS}	V_{CC} = 5.5 V 1/		1, 2, 3	All	-60		mA
Quiescent power supply current (CMOS inputs)	I_{CCQ}	$V_{IN} \le 0.2$ V or $V_{IN} \ge 5.3$ V f_I = 0, V_{CC} = 5.5 V		1, 2, 3	All		1.5	mA
Quiescent power supply current (TTL inputs)	ΔI_{CC}	V_{CC} = 5.5 V, V_{IN} = 3.4 V 2/		1, 2, 3	All		2.0	
Dynamic power supply current	I_{CCD}	V_{CC} = 5.5 V, $V_{IN} \ge 5.3$ V or $V_{IN} \le 0.2$ V, LE = V_{CC}, outputs open, $\overline{OE}$ = GND, one bit toggling - 50% duty cycle		3/	All		0.4	mA/MHz

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{CC} = 5.5 V dc ±10% unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Total power supply current 4/	I_{CC}	V_{CC} = 5.5 V, f_{CP} = 10 Mhz outputs open, $V_{IN} \ge 5.3$ V or $V_{IN} \le 0.2$ V, $\overline{OE}$ = GND, LE = V_{CC}, one bit toggling - 50% duty cycle	1, 2, 3	All		5.5	mA
			1, 2, 3	All		6.0	
Functional tests		See 4.3.1c	7, 8	All			
Input capacitance	C_{IN}	See 4.3.1d	4	All		10	pF
Output capacitance	C_{OUT}	See 4.3.1d	4	All		12	pF
Propagation delay time, D_n to O_n	t_{PLH1}, t_{PHL1}	C_L = 50 pF R_L = 500Ω See figure 4 5/	9,10,11	01	1.0	8.5	ns
				02	1.0	5.6	
Propagation delay time, LE to O_n	t_{PLH2}, t_{PHL2}		9,10,11	01	1.0	15.0	ns
				02	1.0	9.8	
Output enable time	t_{PZH}, t_{PZL}		9,10,11	01	1.0	13.5	ns
				02	1.0	7.5	
Output disable time	t_{PHZ}, t_{PLZ}		9,10,11	01	1.0	10.0	ns
				02	1.0	6.5	

1/ Not more than one output should be shorted at one time and the duration of the short circuit condition should not exceed 1 second.

2/ In accordance with TTL driven input (V_{IN} = 3.4 V dc); all other outputs at V_{CC} or GND.

3/ This parameter is not directly testable, but is derived for use in total power supply calculations.

4/ $I_{CC} = I_{CCQ} + (\Delta I_{CC} \times D_H \times N_T) + (I_{CCD} \times f_I \times N_I)$

Where: D_H = duty cycle for TTL inputs high

N_T = number of TTL inputs at D_H.

f_I = input frequency in Mhz.

N_I = number of inputs at f_I.

5/ Minimum limits shall be guaranteed, if not tested, to the limits of table I.

Device types 01 and 02	
Case outlines	R, S, and 2
Terminal number	Terminal symbol
1	$\overline{OE}$
2	D_0
3	D_1
4	D_2
5	D_3
6	D_4
7	D_5
8	D_6
9	D_7
10	GND
11	LE
12	O_7
13	O_6
14	O_5
15	O_4
16	O_3
17	O_2
18	O_1
19	O_0
20	V_{CC}

FIGURE 1. Terminal connections.

Inputs			Output
D_n	LE	$\overline{OE}$	O_n
H	H	L	H
L	H	L	L
X	X	H	X

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance

FIGURE 2. Truth table.

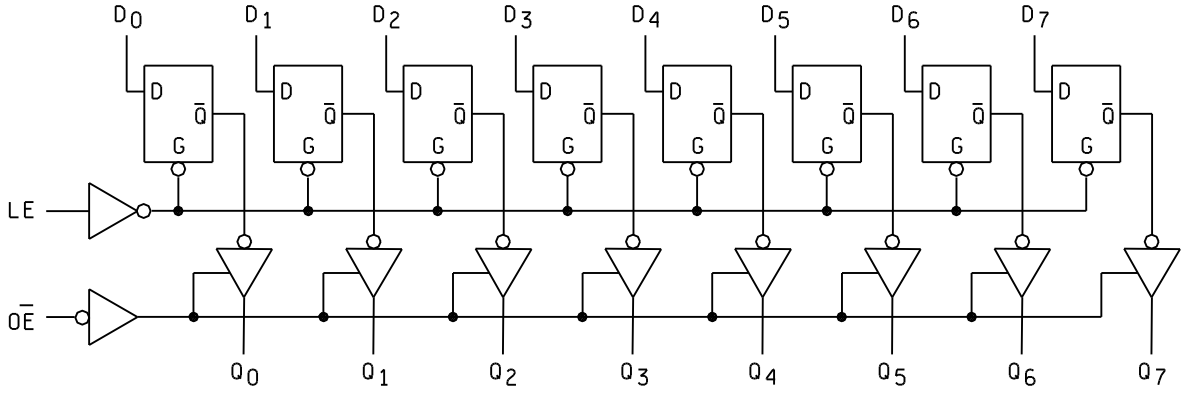
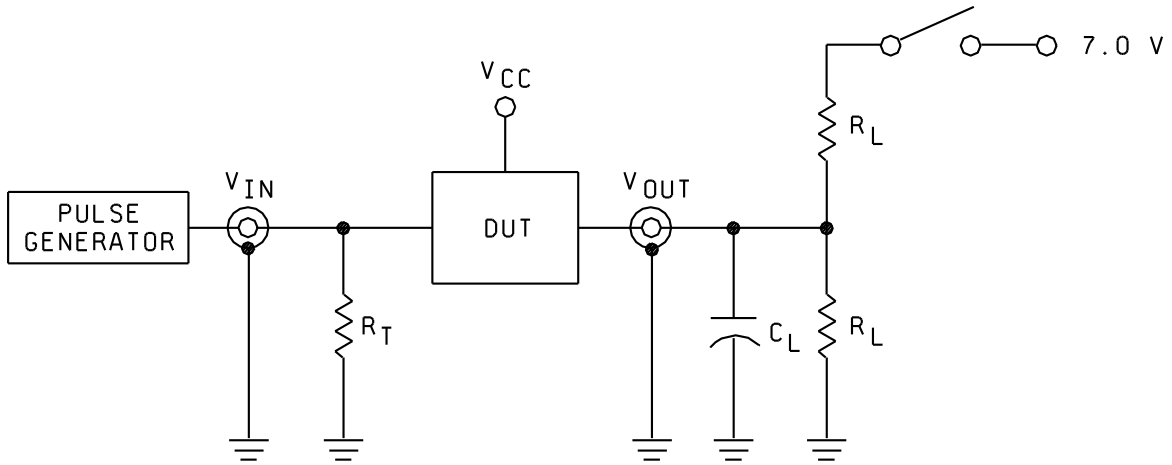


FIGURE 3. Logic diagram.

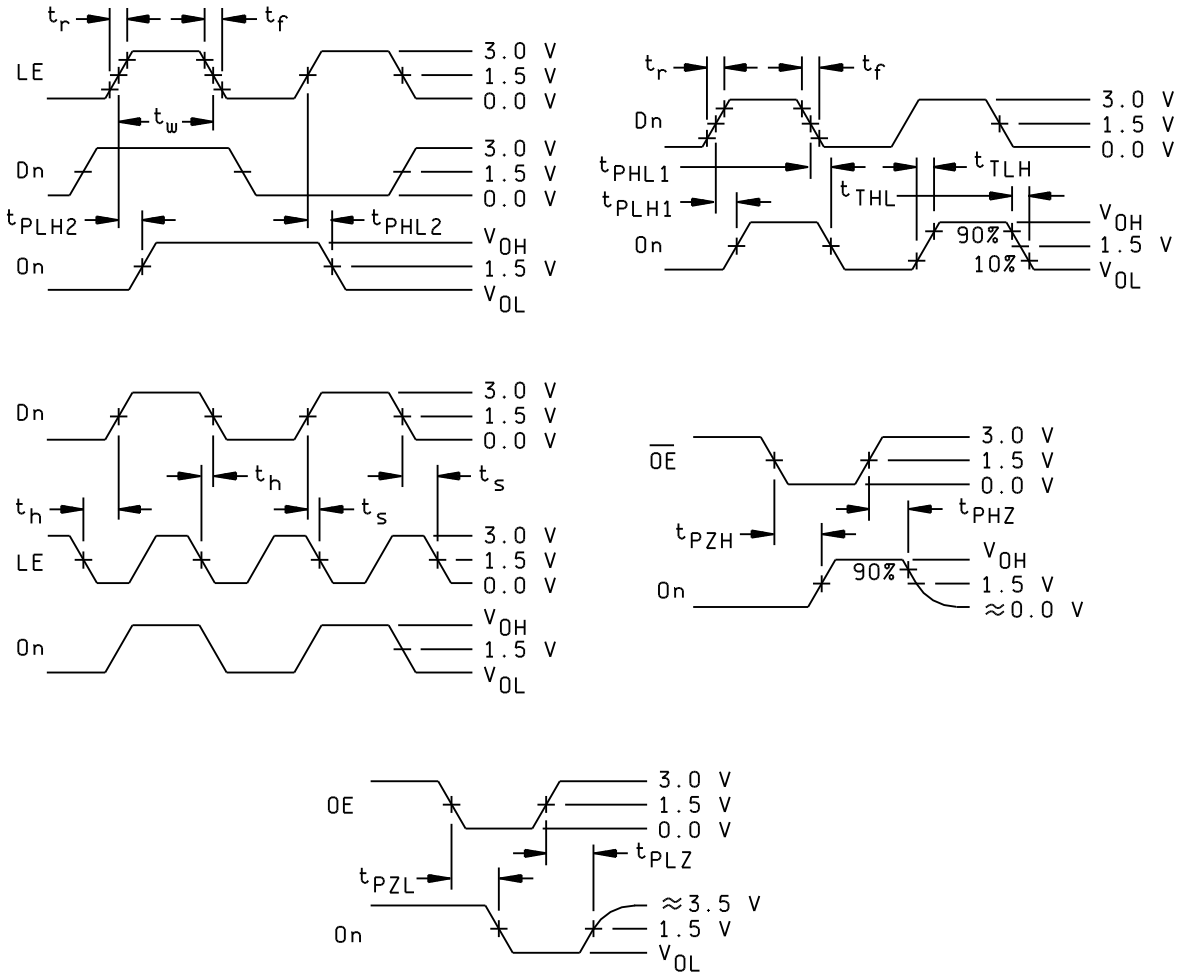


Switch position

Test	Switch
t_{PLZ}	Closed
t_{PZL}	Closed
All other	Open

Definitiions:
R_L = Load resistor (see ac characteristics for value).
C_L = 50 pF, load capacitance includes jig and probe capacitance.
R_T = Termination should be equal to Z_{OUT} of pulse generator.

FIGURE 4. Switching waveforms and test circuit.



NOTE: Input: $t_r = t_f = 2.5$ ns (10% to 90%) unless otherwise specified.

FIGURE 4. Switching waveforms and test circuit - Continued.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-EC shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125° C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroups 7 and 8 shall include verification of the truth table.

d. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial test and after process or design changes which may affect input capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 Mhz. Test all applicable pins on five devices with zero failures.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5005)	1
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 4, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

* PDA applies to subgroup 1.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or Dusing the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125° C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.5 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444, or telephone (513) 296-5377.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.

STANDARDIZED MILITARY DRAWING SOURCE APPROVAL BULLETIN

DATE: 91-04-11

Approved sources of supply for SMD 5962-88639 are listed below for immediate acquisition only and shall be added to MIL-BUL-103 during the next revision. MIL-BUL-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DESC-EC. This bulletin is superseded by the next dated revision of MIL-BUL-103.

Standardized military drawing PIN	Vendor CAGE number	Vendor similar PIN 1/
5962-8863901RX	27014 61772 75569	54FCT573DMQB IDT54FCT573DB P54PCT573DMB
5962-8863901SX	27014 61772	54FCT573FMQB IDT54FCT573EB
5962-88639012X	27014 61772	54FCT573LMQB IDT54FCT573LB
5962-8863902RX	61772 75569	IDT54FCT573ADB P54PCT573ADMB
5962-8863902SX	61772	IDT54FCT573AEB
5962-88639022X	61772	IDT54FCT573ALB

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
27014	National Semiconductor 2900 Semiconductor Drive P.O. Box 58096 Santa Clara, CA 95052-8090
61772	Integrated Device Technology 3236 Scott Boulevard Santa Clara, CA 95052
75569	Performance Semiconductor 610 East Weddell Drive Sunnyvale, CT 94089